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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/790,296	03/01/2004	Khoi A. Phan	H1907 / AMDP986US	9254

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EXAMINER	
DINH, PAUL	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 09/16/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary	Application No.	Applicant(s)	
	10/790,296	PHAN ET AL.	
	Examiner	Art Unit	
	Paul Dinh	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 August 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-27 and 29-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-27 and 29-34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Paul Dinh

Attachment(s)

1) ☐ Notice of References Cited (PTO-892) None
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This FINAL office action is a response to the amendment + remarks filed on 8/31/05.

The amendment does not overcome prior art of record and the remarks are not persuasive; therefor, the rejections based on Mieher are retained.

Claims 1, 3-27, and 29-34 are pending

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form The basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) The invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 3-27, and 29-34 are rejected under 35 U.S.C. 102(e) as being anticipated by the prior art of record Mieher et al (US patent Application Publication No. 2004/0257571)

(Claim 1 and similarly recited claims 23, 33, and 34)

An overlay target (see one or more of: i.e., abstract, fig 9a, fig 15, para. 0029-0030, 0095, 0176, 0210, 0219, 0290) that represents overlay between three or more layers of a wafer (para 0105, 0290) and

A measurement (one or more of: fig 2-5, 7-8, 14) component that determines overlay error existent in the overlay target, and thereby determines overlay error between the three or more layers of the wafer, where the measurement component a comparison component that compares a captured signature with one or more stored signatures to determine overlay error existent in the overlay target (one or more of: para 0020, 0090, 0092, 0102, 0139, 0234-0235, fig 3-15)

A control component or correction of overlay error step (control component or correction of overlay error step = automated process control system in para 0306) that utilizes the overlay error determined by the measurement component to correct overlay error (para 0306) between the three or more layers (para 0105, 0290) of the wafer.

(Claim 3) the control component provides more correction in a first dimension and less correction in a second dimension in an instance in which design rule requirements tolerate less overlay error in the first dimension when compared to the second dimension (fig 13-14, i.e., depend on level of dimension tolerance (para. 0052) and/or how critical the dimensions are (para. 0029, 0296)).

(Claims 4-5) a substantial/insubstantial overlay correction between non-adjacent layers of the wafer in a first dimension correlates to a substantial/insubstantial overlay correction between adjacent layers of the wafer in a second dimension (fig 2-15).

(Claims 6-7, 26) wherein the control component manipulates at least one of temperature(s) associated with a process step, pressure(s) associated with a process step, concentration of gas (es) within a process step, concentration of chemical(s) within a process step, composition of gas (es) within a process step, composition of chemical(s) within a process step, flow rate of gas (es) within a process step, flow rate of chemical(s) within a process step, timing parameters associated with a process step, and excitation of voltages associated with a process step (fig 2-15), wherein at least one of concentration, rate of flow, and degree of abrasiveness is controlled to correct overlay error (fig 2-13).

(Claim 8) the control component facilitates correction of rotational overlay error (one or more of: para. 0103-0104, 0107, 0150, 0187, 0193-0194, 0235, 0259, 0274)

(Claim 9) the measurement component and the control component are integrated with at least one process step to facilitate in situ correction of overlay error (fig 2-15 in combination with other processes/hardware/software/steps forming in situ)

(Claims 10, 32) the control component facilitating simultaneous overlay correction of two or more wafers (para 0110, 0259, 0306).

(Claim 11) the overlay target has a structure of at least one of box-in-box, frame-in-frame, segmented frame, and periodic structure (one or more of: para 0019, 0093 0110, 0120, 1030, 0247, 0278, 0282, 0284, fig 5E, 9, 11-12).

(Claim 12) the overlay target comprises one or more gratings (one or more of: para 0030, 0093-0094, 0123, 1028, 0150, 0210, 0232, fig 8, 15)

(Claim 13) the measuring comparing an optical microscope utilized to capture an image of the overlay target (fig 4-10)

(Claim 14) the measurement component further comprising a light emitting component that delivers light incident to the overlay target (one or more of: para 0013-0014, 0106, 0115, 0142, 0152, 0230-0235, fig 4-15); and a light capturing component to capture a signature that results from the incident light contacting the overlay target (one or more of: para 0013-0014, 0278, 0106, 0115, 0142, 0152, 0230-0235, fig 4-15)

(Claim 15) optical microscopy techniques are utilized to facilitate measurement of overlay error existent in the overlay target (fig 5-15, para 0128, 0143, 0207, 0263)

(Claims 16, 18) scatterometry technique are utilized to facilitate measurement of overlay error existent in the overlay target (title, abstract, para 0008-0021, 0290, fig 8, 11), Fourier transform infrared scatterometry (title, para 0029) technique are utilized to facilitate measurement of overlay error existent in the overlay target (one or more of: abstract, para 0008-0021, 0098, 0129, 0164, 0172, 0174, 0210, fig 8, 11)

(Claim 17) SEM techniques are utilized to facilitate measurement of overlay error existent in the overlay target (one or more of: para 0029, 0207, 0238, 0296, 0299, 0301-0303)

(Claims 19, 24) a stand-alone metrology (one or more of: fig 7, 13-15, para. 0027, 0029, 1019-0110, 0114, 0126, 0220, 0242, 0250-0256)

(Claim 20) the overlay target associated with a particular die on the wafer (one or more of: fig 1-15).

(Claim 21) the wafer subdivided into a grid (para 0106) comprising a plurality of cells, wherein the grid facilitates measurement and recordation of overlay error at particular portions of the wafer

(Claim 22) the wafer discarded if a threshold percentage of cells exhibit a threshold level of overlay error (one or more of: para 0101, 0218, 0255, 0257, fig 2-15).

(Claim 25) correcting overlay error between non-adjacent layers of the wafer based at least in part on the measured overlay error existent in representative layers of the overlay target (para 0105, 0290, 0306)

(Claim 27) further comprising approximating overlay error between adjacent layers on a wafer via measuring overlay error between the representative layers of the overlay target (one or more of: para 0105, 0290, 0306, fig 2-15)

(Claims 29-30) substantially/insubstantially correcting overlay error between non-adjacent layers of the wafer in a first dimension (para 0105, 0290, 0306, fig 2-15), and substantially/insubstantially correcting overlay error between adjacent layers of the wafer in a second dimension (one or more of: para 0105, 0290, 0296, 0306, fig 2-15)

(Claim 31) further comprising providing a greater amount of overlay correction in one particular direction in comparison to a substantially perpendicular dimension (para 0029).

Response to Applicant Remarks

The applicant state that Mieher does not discloses "**a control component or correction of overlay error step**, a limitation that included in independent claims 1, 23, 33, and 34 of subject invention"

Here are examiner answers:

As detailed above, Mieher does not disclose a control component or correction of overlay error step (**control component or correction of overlay error step = automated process control system in para 0306**) that utilizes the overlay error determined by the measurement component to correct overlay error (para 0306) between the three or more layers (para 0105, 0290) of the wafer.

The following is para. 0306 that discloses the **control component or correction of overlay error step** in independent claims 1, 23, 33, and 34 of subject invention

"[0306] The overlay results obtained with scatterometry overlay techniques described herein, including the linear differential method and phase-detection algorithms, may be used to calculate **corrections** to the stepper settings **to minimize overlay error**. These calculated corrections for lithography steppers or scanners are commonly referred to as "stepper correctables." The stepper **correctables obtained from scatterometry overlay measurements may be used as inputs to the stepper to minimize overlay error for subsequent wafer processing**. The **overlay errors or stepper correctables obtained from scatterometry overlay may be input to an automated process control system which may then calculate a set of stepper corrections to input to the stepper to minimize the overlay errors for subsequent wafer processing**. The **overlay errors, stepper correctables, or calculated**

worst overlay errors on the wafer obtained with scatterometry overlay may be used to disposition product wafers to decide if the wafer requires rework or meets overlay requirements for further wafer processing"

and "three or more layers" is disclosed in para 0105 ("more that two layers"), para 0290 (layers L1-L3)

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul Dinh whose telephone number is 571-272-1890. The examiner can normally be reached on Monday to Friday from 8:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S. Smith can be reached on 571-272-1907. The fax number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Paul Dinh
Patent Examiner